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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 09/131,846
Filing Date: July 24, 1998
Appellant(s): DENNING ET AL.

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For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed September 18th, 2001.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-18 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,701,409	Gates	12-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-18 stand rejected under 35 U.S.C. §102 (e). This rejection is set forth in prior Office Action, Paper No. 6.

(11) Response to Argument

In defense of the Final Rejection under 35 USC §102(e), the Examiner will first describe the Gates reference in light of the Applicant's remarks throughout prosecution of the present application.

Gates has described a system which generates an invalid parity (an error generated most commonly in hardware) and places this parity on a bus (specifically a

PCI, a series of copper wires connected to a variety of expansion components in a computer). Parity is a digital abstraction used in error correction and coding indicating the binary values of a message have been altered. This parity data (digital data) is then placed on the PCI. As parity is a digital abstraction it can not be physically placed on copper wires. A series of high and low voltage pulses are used to charge the PCI bus to transmit this data. The nature of this signal is the point of contention between Applicant and the Office.

First, Applicant contends that Gates fails to disclose a digital-to-analog converter. This is immaterial as Applicant does not positively recite a digital-to-analog converter in the independent claims.

Second, Applicant contends that phrase "analog voltage signal" obviates Gates from any applicability in any manner in the present application. Applicant has provided the definitions of analog and digital for consideration before the Board which the Examiner accepts. While Applicant has clearly analog properties, the contrasting with a digital seems to confuse the issue as Gates does not teach a "digital voltage signal". Given that both Applicant and Gates use the PCI bus architecture, it unclear how the fundamental physical properties of the voltage driven on bus line can differ, let alone have Gates be a physical impossibility in the context of the current application..

Third, Applicant contends even if the voltage is analog, Gates continues to fail to teach the creation of an analog voltage signal representing a hardware fault. As described above, Gates simulates a specific type of hardware fault, a parity error. Once the configuration of a parity error is created, this series of signals (commonly called a

signature) must be placed on the bus. While parity is in fact a digital data concept, the copper wires of a PCI only transmit voltages defined by Applicant specifically as analog. As such a series of transistors must drive the analog voltage in such a manner that the digital data signal is transmitted across the PCI bus.

Additionally, Applicant's statements concerning logical "ones" and "zeros" not even being even being intimated at in the most rudimentary degree within Gates, is cause for concern, as logical "ones" and "zeros" (also known as digital "highs" and "lows" within Gates) are physically manifested by analog voltage signals on a PCI bus. Further, parity is series of logical operations and thus inherently requires logical "ones" and "zeros".

In summary, it is the contention of the Examiner that a digital data signal with an accompanying parity data conveyed in an analog voltage signal on a metal wire PCI bus as taught by Gates is encompassed by the breadth of Applicant present claims.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Bryce P. Bonzo

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October 15, 2001

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